IN THE SPECIFICATION:

Please replace the following paragraphs with the below written paragraphs:

The paragraph beginning on page 6, line 19:

A clock reception/distribution unit 203 receives the FP2 and CP2 signals inputted from the LTRIA 300 to the TSCMA 200 to distribute the synchronization pulses and clock signals selected in the same way for each doubled board among the boards. An RS-485 device 205 receives the signals from the TDCMA 400 and interfaces through a DS-BUS I/F 209, and the received signals are also stored in a buffer 206 for a subsequent transmission to a System Address/Data Bus (SADL) 217.

The paragraph beginning on page 7, line 8:

A Tx control memory combiner 211 comprises a voice memory device and control memory device serve to switch 16.384 Mbps voice data of 2K time slot inputted from the SMDXA 100 at maximum 8K time slot in the inter-direction (S-Switch or Host system) and intra-direction. Here, the switched PCM data may be transferred to the inter-direction (S-Switch), or looped to an Rx control memory combiner 213. In addition, the 2K time slot PCM data in the intra-direction is demultiplexed in the outside of the memory module with the even 1K for the intra-looping and the odd 1K to the additional services. A Dumx 223 is provided to receive the output of the Tx control memory combiner 211.

The Rx control memory combiner 213 switches the 2K time slot PCM data inputted from the LTRIA 300, and the 2K time slot PCM data formed through the inter-path. The LTRIA 300 may contain at maximum 4K-time slot, and transmit the switched PCM data at maximum 8K-

time slot to the SMDXA 100 in the LVDS level. A time slot-rearranging unit 215 rearranges the time slot of the intra-switched PCM data. A Mux 225 is coupled to receive the output of the time slot-rearranging unit 215, and the output of the Mux 225 is transmitted to a tone bert 229 for conversion or to a bit error–rate test.